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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FISH & RICHARDSON, PC 12390 EL CAMINO REAL SAN DIEGO, CA 92130-2081			EXAMINER SHINGLETON, MICHAEL B	
			ART UNIT 2817	PAPER NUMBER

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.



## Office Action Summary

**Application No.**

10/695,262

**Applicant(s)**

SENTHILKUMAR ET AL.

**Examiner**

Michael B. Shingleton

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 21-23 and 28-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 21-23 and 28-44 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>7/7/2004</u> | 6) <input type="checkbox"/> Other: ____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 21, 33, 34, 39 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. 4,977,380 (Martin) in view of Klughart 5,546,055 (Klughart '055).

Figures 4, 5a and 5b in combination with the entire disclosure of Martin disclose an apparatus/method for providing a variable level of capacitance having a plurality of capacitors (C13, C14...), each selectable through an independent control signal (In Figures 4 and 5b of Martin. Note the signal lines individually connected to the gates of the switching elements like Q14 that control which capacitor is connected in or out of the circuit.). These independent control signals are generated by a logic circuit (Note Figure 5a that clearly shows logic elements like U6A, U6B that forms a logic circuit.). The selected capacitors of Martin clearly provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors. Martin also clearly discloses buffer circuitry (Note Figure 5b that shows the use of buffer circuitry like U9E. Also note column 4, around line 21 that describes these elements as "buffers"). These buffers inherently isolate. Thus in the circuit of Martin these buffers decouple the plurality of capacitors from the logic circuit that clearly prevents noise in the logic circuit from affecting the plurality of capacitors. Martin however is silent on the exact composition of the capacitors and specifically the use of MOSFET capacitors.

Figure 9 of Klughart '055 discloses the use of on-chip n-depletion MOSFET load capacitors 1230 and 1232 whose source and drain are clearly connected together as is clearly illustrated. Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '055.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip n-depletion MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors of Martin because, as the Martin reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-

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recognized equivalent capacitor such as the well-known on-chip n-depletion MOSFET capacitors as recited by Klughart '055.

The combination above is silent on the exact values of the capacitors that make up the capacitor bank. Specifically having at least one that is less than 1 pF.

However, the selection of the capacitance values is merely part of the optimum or workable range. The values of the capacitors determines how many are needed and how great a resolution one can obtain which is all part of the selection of optimum or workable range.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have selected the value of at least one of the capacitances in the combination above to be less than one pico-Farad (PF) as this is the selection of the optimum or workable range that involves but routine skill in the art.

Claims 21, 22, 29, 30, 39-42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke in view of Ochiai et al. US 4,851,792 (Ochiai), Klughart '055 and Horn "Basic Electronics Theory" 4th Edition pp 377-378, pp 418-426 and pp 454-465.

The oscillator circuit of Clarke includes a capacitor circuit that includes a plurality of on-chip capacitors C1-C6. Each of these capacitors is independently selectable by a control signal D0-D5. The amount of the capacitance is clearly a function of how many capacitors are connected. The voltage signal  $V_{bias}$  is considered by Clarke to be a bias voltage signal and it is applied to the capacitors C1-C6 via a resistor element 33. Clarke is silent on the composition of the on-chip capacitors. Clarke is also silent on using buffer circuitry to decouple the transmission gate switches from the set of memory registers. Clarke is silent on the use of a filtered power supply for the bias source of the capacitors.

Figure 9 of Klughart '055 discloses the use of on-chip n-depletion MOSFET load capacitors 1230 and 1232 whose source and drain are clearly connected together as is clearly illustrated. Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '055.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip n-depletion MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors C1-C6 of Clarke wherein each of these capacitors C1-C6 has a terminal connected to ground because, as the Clarke reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip n-depletion MOSFET capacitors as recited by Klughart '055 for the capacitors of Clarke.

Figure 8(a) of Ochiai discloses a biasing arrangement for the capacitors of an oscillator and is configured such that the bias voltage  $V_B$  of the capacitor 14 “remains constant” (See column 5 around line 61 of Ochiai). This as recognized by Ochiai allows for the oscillation frequency to remain constant. It is conventionally known that changes of bias to a MOS type capacitor including MOSFET based MOS capacitors will cause changes in its capacitance much like a pin arrangement. It is the teaching of Clarke to have capacitors C1-C6 to be capacitors having discrete i.e. non-changing values. Clarke obtains the change in capacitance by switching these capacitors of discrete values in and out of the circuit. Clarke shows and describes no means by which the individual capacitances of these capacitors are changed.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the oscillator arrangement of Clarke and Klughart ‘055 with a bias arrangement that keeps the necessary bias voltage of the capacitor elements constant so as to prevent the individual capacitance elements from varying in capacitance and thus preventing an undesirable drift in oscillator frequency as taught by Ochiai.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces “ripple”, i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the filtered power supply made obvious above to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Claims 21, 22, 31, 32, 39, 40-42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke 6,337,604 (Clarke) in view Ochiai et al. US 4,851,792 (Ochiai), Klughart US 5,801,411 (Klughart ‘411) and Horn “Basic Electronics Theory” 4th Edition pp 377-378, pp 418-426 and pp 454-465.

The oscillator circuit of Clarke includes a capacitor circuit that includes a plurality of on-chip capacitors C1-C6. Each of these capacitors is independently selectable by a control signal D0-D5. The

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amount of the capacitance is clearly a function of how many capacitors are connected. The voltage signal  $V_{bias}$  is considered by Clarke to be a bias voltage signal and it is applied to the capacitors C1-C6 via a resistor element 33. Clarke is silent on the composition of the on-chip capacitors. Clarke is also silent on using buffer circuitry to decouple the transmission gate switches from the set of memory registers. Clarke is silent on the use of a filtered power supply for the bias source of the capacitors.

Figure 9b of Klughart '411 discloses the use of on-chip p-enhancement MOSFET capacitor 32 whose source and drain are clearly connected together as "common" i.e. conventional (See column 7, around line 18). Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '411.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip p-enhancement MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors C1-C6 of Clarke wherein each of these capacitors C1-C6 has a terminal connected to ground because, as the Clarke reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip p-enhancement MOSFET capacitors as recited by Klughart '411 for the capacitors of Clarke.

Figure 8(a) of Ochiai discloses a biasing arrangement for the capacitors of an oscillator and is configured such that the bias voltage VB of the capacitor 14 "remains constant" (See column 5 around line 61 of Ochiai). This as recognized by Ochiai allows for the oscillation frequency to remain constant. It is conventionally known that changes of bias to a MOS type capacitor including MOSFET based MOS capacitors will cause changes in its capacitance much like a pin arrangement. It is the teaching of Clarke to have capacitors C1-C6 to be capacitors having discrete i.e. non-changing values. Clarke obtains the change in capacitance by switching these capacitors of discrete values in and out of the circuit. Clarke shows and describes no means by which the individual capacitances of these capacitors are changed.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the oscillator arrangement of Clarke and Klughart '055 with a bias arrangement that keeps the necessary bias voltage of the capacitor elements constant so as to prevent the individual capacitance elements from varying in capacitance and thus preventing an undesirable drift in oscillator frequency as taught by Ochiai.

Horn teaches that buffers are used to ensure that the output drive is sufficient to drive the devices on the output thereof.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a buffers between the transmission gate switches and the memory registers so as to insure that there is sufficient drive for the transmission gate switches as taught by Horn.

Clarke is likewise silent on the use of filtered power signals to power the buffer circuitry. Buffer circuitry requires a power supply as is well known in the art so that it can provide the sufficient drive as noted above. Horn teaches that it is commonplace to utilize filtered power supplies, in particular note pages 456 and 460 to power electronic devices. This as Horn recognizes reduces “ripple”, i.e. noise, or voltage fluctuations that then in turn causes less vacillations in the devices powered by such power supplies.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the filtered power supply made obvious above to power the buffers made obvious above so as to reduce the introduction of noise in the system as is taught by Horn.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. 4,977,380 (Martin) in view of Morand et al. 6,734,483 (Morand).

Figures 4, 5a and 5b in combination with the entire disclosure of Martin disclose an apparatus/method for providing a variable level of capacitance having a plurality of capacitors (C13, C14...), each selectable through an independent control signal (In Figures 4 and 5b of Martin. Note the signal lines individually connected to the gates of the switching elements like Q14 that control which capacitor is connected in or out of the circuit.). These independent control signals are generated by a logic circuit (Note Figure 5a that clearly shows logic elements like U6A, U6B that forms a logic circuit.). The selected capacitors of Martin clearly provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors. Martin also clearly discloses buffer circuitry (Note Figure 5b that shows the use of buffer circuitry like U9E. Also note column 4, around line 21 that describes these elements as “buffers”). These buffers inherently isolate. Thus in the circuit of Martin these buffers decouple the plurality of capacitors from the logic circuit that clearly prevents noise in the logic circuit from affecting the plurality of capacitors. Martin however is silent on the integration of the circuit and exact composition of the capacitors and specifically the use of on-chip metal or on-chip poly capacitors.

To integrate a circuit is well known to save space and make for a more reliable structure. This is further supported by Morand that teaches the use for poly capacitors to be included in an integrated circuit. See column 1 around line 19 of Morand.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip poly capacitors in place of the generic capacitors of Martin because, as the Martin reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known poly capacitor as recited by Morand. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have integrated the circuit of Martin so as to save space and make for a more reliable structure as is well known in the art and as taught by Morand.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin and Morand as applied to claim 35 above, and further in view of Yamazaki et al. 6,181,184 (Yamazaki).

Martin is silent on the showing of the power supply for the buffers and the use of a filter circuit connected to the power supply to generate a filtered power supply signal that is used to power these buffers.

Buffers need a power supply in order to function. Even though the power supply is not shown in Martin one of ordinary skill would have realized that a power supply is required to make the invention work. Figure 39 of Yamazaki shows a power supply Vcc and a filter connected between this power supply and the buffer 122. This not only provides the necessary power to operate a buffer, but the filter clearly filters out the noise or the ac component from and to the power supply.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided both a power supply and a filter in the power supply path for the buffers of Martin so as to provide the necessary power for the buffer as is conventionally known and filter out unwanted signals as taught by Yamazaki.

Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin and Morand as applied to claim 35 above, and further in view of Early et al. 5,391,999 (Early).

As noted above Martin utilizes MOSFETs for the switching elements that switch in and out the capacitors that make up the variable capacitor of Martin. Martin is silent on the use of "transmission gates" for the switching elements.

Early discloses that the shown N-channel transistors (MOSFETs) and the shown Transmission gates are switching elements and that many different elements may be substituted therefore (See the paragraph that begins around line 37). Thus Early clearly recognizes the art recognized



equivalence of these elements as well as the equivalence of these elements with many other forms of switching devices.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted transmission gates for the MOSFETs of Martin. One of ordinary skill in the art would have been motivated to make the substitution for these are art recognized equivalent forms of switches that can be used in place of one another as recognized and taught by Early.

Claims 21, 31, 34, 39 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. 4,977,380 (Martin) in view of Klughart 5,801,411 (Klughart '411).

Figures 4, 5a and 5b in combination with the entire disclosure of Martin disclose an apparatus/method for providing a variable level of capacitance having a plurality of capacitors (C13, C14...), each selectable through an independent control signal (In Figures 4 and 5b of Martin. Note the signal lines individually connected to the gates of the switching elements like Q14 that control which capacitor is connected in or out of the circuit.). These independent control signals are generated by a logic circuit (Note Figure 5a that clearly shows logic elements like U6A, U6B that forms a logic circuit.). The selected capacitors of Martin clearly provide an amount of capacitance that is the sum of the individual capacitances of the selected capacitors. Martin also clearly discloses buffer circuitry (Note Figure 5b that shows the use of buffer circuitry like U9E. Also note column 4, around line 21 that describes these elements as "buffers"). These buffers inherently isolate. Thus in the circuit of Martin these buffers decouple the plurality of capacitors from the logic circuit that clearly prevents noise in the logic circuit from affecting the plurality of capacitors. Martin however is silent on the exact composition of the capacitors and specifically the use of MOSFET capacitors.

Figure 9b of Klughart '411 discloses the use of on-chip p-enhancement MOSFET capacitor 32 whose source and drain are clearly connected together as "common" i.e. conventional (See column 7, around line 18). Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '411.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip p-enhancement MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors Martin because, as the Martin reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip p-enhancement MOSFET capacitors as recited by Klughart '411.

The combination above is silent on the exact values of the capacitors that make up the capacitor bank. Specifically having one that is less than 1 pF.

However, the selection of the capacitance values is merely part of the optimum or workable range. The values of the capacitors determines how many are needed and how great a resolution one can obtain which is all part of the selection of optimum or workable range.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have selected the value of at least one of the capacitances in the combination above to be less than one pico-Farad (PF) as this is the selection of the optimum or workable range that involves but routine skill in the art.

Claims 22 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin and Klughart '055 as applied to claim 21, 33, 34, 39 and 44 above, and further in view of Yamazaki et al. 6,181,184 (Yamazaki).

Martin is silent on the showing of the power supply for the buffers and the use of a filter circuit connected to the power supply to generate a filtered power supply signal that is used to power these buffers.

Buffers need a power supply in order to function. Even though the power supply is not shown in Martin one of ordinary skill would have realized that a power supply is required to make the invention work. Figure 39 of Yamazaki shows a power supply Vcc and a filter connected between this power supply and the buffer 122. This not only provides the necessary power to operate a buffer, but the filter clearly filters out the noise or the ac component from and to the power supply.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided both a power supply and a filter in the power supply path for the buffers of Martin so as to provide the necessary power for the buffer as is conventionally known and filter out unwanted signals as taught by Yamazaki.

Claims 23 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin and Klughart '055 as applied to claim 21, 33, 34, 39 and 44 above, and further in view of Early et al. 5,391,999 (Early).

As noted above Martin utilizes MOSFETs for the switching elements that switch in and out the capacitors that make up the variable capacitor of Martin. Martin is silent on the use of "transmission gates" for the switching elements.

Early discloses that the shown N-channel transistors (MOSFETs) and the shown

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Transmission gates are switching elements and that many different elements may be substituted therefore (See the paragraph that begins around line 37). Thus Early clearly recognizes the art recognized equivalence of these elements as well as the equivalence of these elements with many other forms of switching devices.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted transmission gates for the MOSFETs of Martin. One of ordinary skill in the art would have been motivated to make the substitution for these are art recognized equivalent forms of switches that can be used in place of one another as recognized and taught by Early.

Applicant's arguments with respect to claims 21-23 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770. The examiner can normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Fridays. The examiner normally has second Fridays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS

March 25, 2004

December 22, 2004

*Michael B. Shingleton*  
**MICHAEL B. SHINGLETON**  
**PRIMARY EXAMINER**  
**GROUP ART UNIT 2817**

